A Harmonic Elimination Method For Three-Phase PWM Rectifier To Reduce Computational Complexity

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***Abstract*— Proportional integral (PI) or proportional resonant (PR) controller are the most popular controllers used to shape the current of voltage sourced converters. Besides, current harmonics are inevitably generated while using a three-phase PWM rectifiers. Since the bandwidth of the controller is usually not fast enough to compensate for the generated harmonics, the harmonics are not removed. Selective harmonic compensation is the most popular for compensation of hormoics. This approach, however, needs a significant time for its calculations, as elimination of each harmonic requires its resonant filter. Moreover, to utilize the average current mode technique, the switching frequency of the converter should be synchronized with the sampling frequency of the analog to digital converter (ADC), and the bandwidth of the current controller, as a rule of thumb, should be limited to one-tenth of the switching frequency. This paper proposes a novel elimination approach which suppresses the harmonics by fewer strive and provides sufficient bandwidth for the controller to be able to eliminate the higher-order harmonics. The proposed method is experimentally verified on a 10 KW three-phase PWM rectifier.**

Keywords— elimination of harmonics, compensation, digital control

I. INTRODUCTION

Voltage sourced rectifiers are very popular in HVDC systems, active filters, and high voltage data centers [1,2,3]. Traditionally, a three-phase PWM rectifier consists of a three-phase active bridge, a DC bus capacitor, and three AC-side inductors as shown in Fig. 1. The amplitude and phase angle of the currents flowing through the AC side is regulated using a current control loop. This controller determines the voltage of the three-phase bridge such that the voltage difference across each AC-side inductor results in AC current in the inductor to be in-phase with the line voltage. Nowadays non-linear loads are extensively used. These loads draw non-sinusoidal current from the grid and induce harmonic current in the grid which distorts the grid voltage. The line voltage harmonics can distort the sinusoidal currents into PWM rectifiers. As the AC-side inductors have small values, even small line voltage harmonics may cause existence of distortions unless the PWM bridge voltage could be controlled such that it creates counterpart voltage harmonics. However, speed of the controller of current loop in voltage sourced converters is typically little. Therefore, different order voltage distortions surpass the speed of the control loop. So the current controller is not able to compensate the line voltage harmonics and considerable current harmonics are generated when the grid voltage is contaminated with harmonics. To eliminate the current harmonics, various approaches have been proposed [4-8]. The selective harmonic compensation concept applies resonant filters for each harmonic [6, 7, 8]. In this way, adequate gain is provided for the controller to eliminate the particular harmonic. With this method any particular harmonic requires its compensator, hence many effort is needed to be made by the processor. [6] and [7] use a synchronous reference frame resonant controller for each harmonic (either a positive sequence harmonic or a negative sequence one). In [8] the authors have compared different harmonic elimination techniques, i.e. compensating in; the stationary reference frame, the rotating reference frame, and multiple rotating reference frames. In all the mentioned methods multiple resonant filters are used for compensation and need a considerable computation effort. In [10] the author suggests simplifying this computational burden by compensating for the harmonics in the synchronous reference frame such that two harmonics can be compensated using one resonant filter. For instance, if one considers a reference frame that is rotating with ω_1 , a resonant filter at $6\omega_1$ frequency can eliminate both 5th and 7th order harmonics [16]. In [17] the author introduces an approach that individually detects the specific order harmonic in each individual harmonic control loop. In this way, each harmonic is separately removed by its filter; nevertheless, it still imposes a considerable computation effort on Digital Signal Processor (DSP). Using these harmonic elimination methods, the bandwidth of the current controller should be large enough to cover the frequency of all the harmonics; otherwise, the current controller might lead to instability [11].

This paper takes advantage of the new harmonic elimination method that recently presented by the authors in [13]. In [13] samples of system current are taken into account, and after filtering out the harmonics from it, using a low pass

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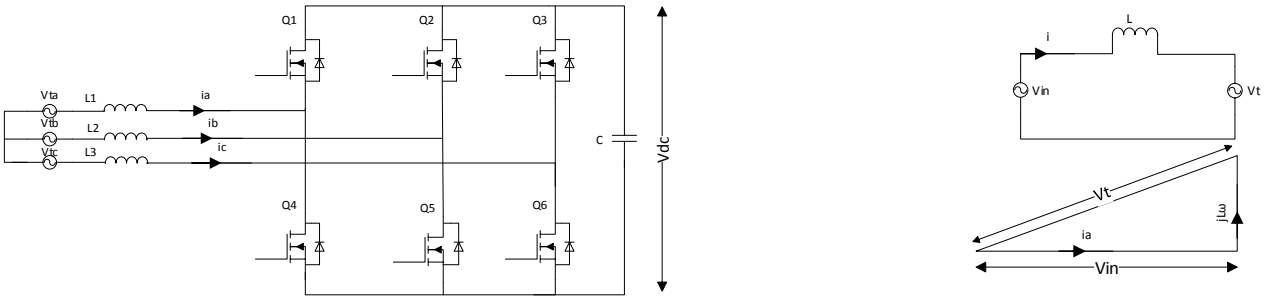

(a) (b)

Fig. 1 (a). diagrammatic voltage sourced converter, Fig. 1 (b). Phasor analysis associated with harmonic generation

filter, they are again added to system current. The proposed approach leads to less amount of computation for the processor. Section II presents a comprehensive description of the harmonic generation and current control in PWM rectifiers. Section III discusses the limitations of digital signal processors in digital control of power electronic converters and illustrates how the digital control of power electronic devices can affect the phase margin and bandwidth of the systems. Next, in section IV the corresponding transfer function for the implemented harmonic elimination approach is obtained. Section V describes the overview of the methodology for the implementation of the newly presented harmonic elimination method. The presented method is implemented on a three-phase PWM rectifier and experimental results illustrate how computation time is saved using the presented harmonic elimination method.

II. CURRENT HARMONICS IN THREE-PHASE PWM RECTIFIER

The current of the PWM rectifiers are usually polluted by harmonics. In this section the origin of current harmonics generation in PWM rectifiers is explained, then the conventional control approaches that are used to control the PWM rectifier and to eliminate harmonics are discussed.

A. Origin of current harmonics

The stem of the generated current harmonics in PWM rectifiers is in the grid voltage harmonic distortion. This can be shown by performing an analysis of the system shown in Fig. 1(a) in stationary coordinate system [12]. The terminal voltages of the rectifier in the α-β coordinate system are denoted by $V_{t\alpha}$ and $V_{t\beta}$.

$$\begin{bmatrix} V_{t\alpha} \\ V_{t\beta} \end{bmatrix} = \begin{bmatrix} Q_\alpha \\ Q_\beta \end{bmatrix} V_{dc} \tag{1}$$

Where Q_α and Q_b are defined based on the Clarke transform of gate command signals of the switchesQ_1, Q_2 and Q_3

$$\begin{bmatrix} Q_\alpha \\ Q_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \end{bmatrix} \tag{2}$$

The positive sequence component of $V_{t\alpha}$, $V_{t\beta}$ and the h^{th} harmonic component of the grid voltage on a normalized time base can be obtained as:

$$V_t^{+1} = \frac{1}{2\pi}\int_0^{2\pi}\left(V_{t\alpha} + jV_{t\beta}\right)e^{-jt}\,dt \tag{3}$$

$$V_t^h = \frac{1}{2\pi}\int_0^{2\pi}\left(V_{t\alpha} + jV_{t\beta}\right)e^{-jht}\,dt \tag{4}$$

$$(h = -5, +7, -11, +13, \dots)$$

Consequently, by performing a phasor diagram calculation (Fig. 1 (b)), the h^{th} harmonic of the current is calculated:

$$\vec{I}^h = \frac{\vec{V}_s^h - \vec{V}_t^h}{R + j|h|L\omega} \tag{5}$$

Usually *R* and *L* form a small impedance. Considering equation 5, if the harmonic components exist on the grid voltage, the difference between $\vec{V}_s^h$ and $\vec{V}_t^h$ can lead to considerable current harmonics unless the controller compensates that current harmonics at terminal voltage. A fast current controller eliminates the harmonics. However, the bandwidth of the current controllers, either PI or PR, are limited as discussed later in section III.

B. Conventional control and harmonic elimination approaches

The conventional control structure which is used to control currents of the voltage sourced converter is presented in Fig. 2. Depending on the type of the reference frame, i.e. either synchronous or rotational, a proportional intergral or a proportional resonant controller is employed. Besides, a feed-forward signal from grid voltage is typically used to

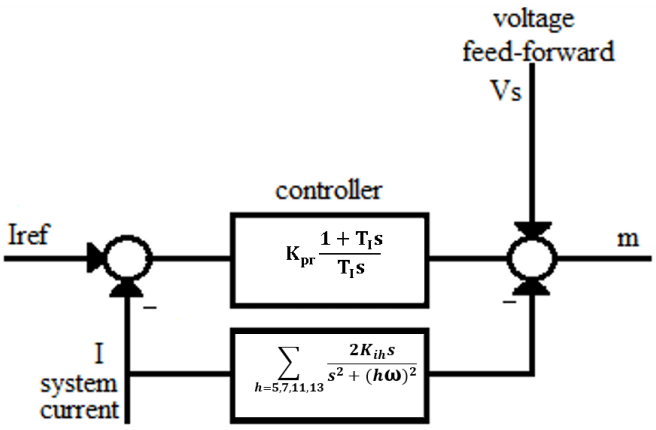

Fig. 2. A typical controller schematic for control of voltage sourced converter

separate the stream among the converter system and the grid to avoid the transients in the startup. Furthermore, the feed-forward act like rejecting the disturbances of the closed-loop system [9].

The elimination of harmonics, in the stationary reference frame, is conventionally done by applying resonant filters on the frequency of each harmonic. In this way, enough gain is provided for the controller at the frequency of that specific order harmonic. This method of harmonic compensation needs a resonant filter for each harmonic. In the case of applying the current controller in the synchronous reference frame, it is possible to eliminate two harmonics with one resonant filter [10]. Using these harmonic elimination methods, the bandwidth of the current controller should be large enough to cover the frequency of the harmonic that is being eliminated [11].

III. LIMITATIONS IN DIGITAL IMPLEMENTATION

The limited bandwidth of the current controllers is the main reason for harmonic distortion in the current of PWM rectifiers [10]. The computation and sampling constraints of the DSP are key restrictions for increasing the bandwidth of current controllers. This section discusses the role of DSP in control of PWM rectifiers and the limitations that the DSP has to overcome, to effectively eliminate the harmonics.

Fig. 3 shows the sampling and analog to digital conversion of the processor used in this application. Current sampling of the processor at its shortest time (T_s), which is synchronized with the switching frequency, is carried out at the zero instant of the PWM binary counter. At this instant, the analog to digital converter (ADC) of the processor takes the "start of conversion command" (SOC). It takes a certain period of time to convert the analog signals to digital. After the conversion has been completed, an interrupt is generated by the processor which alerts the end of conversion (EOC), indicating that the converted signals are ready to be used by the user software. The course from one EOC to the subsequent EOC is known as interrupt service routine of the processor (ISR). The processor is supposed to do all the calculations of the user software in this span, otherwise, a flag named "interrupt service routine overrun" (ISRovr) alerts the failure.

Fig. 4 shows the analog implementation of a PWM modulator. It is obvious that an occurrence of a tiny change in modulation signal $m(t)$ leads to an immediate change in the duty cycle. Conclusively, the amount of delay introduced in the analog implementation of PWM modulated systems is negligible [15]. Switching loss and efficiency are therefore the remaining limiting factors in increasing switching frequency as well as the bandwidth of the current controller. In contrast, if digital control is applied, the controller's speed is slower in comparison to that of analog due to two main reasons, which are Digital delay and limited ISR time of processors. Additionally, digital delay inevitably appears in the digital implementation of control systems. This is due to the fact that if a digital control is implemented, the carrier signal is quantized by a binary counter and the modulation signal is updated at the beginning of each modulation period [14]. Fig. 3 depicts a uniformly sampled pulse width modulator in which the quantization effects have been ignored. The delay is modeled by equation 6, through 8 [14], where $M(s)$ and $V_{MO}(s)$ are the Laplace transform of the modulating signal $m(t)$ and the output of the comparator $V_{mo}(t)$ respectively and c_{pk} is the sampling time of the PWM binary counter. Digital delay can lead to a considerable reduction of the phase margin and bandwidth of the current controller. The digital delay may reduce the gain. In order to compensate for the gain reduction, the bandwidth should be reduced. Besides, the sampling frequency of the current signal is limited due to the limited ISR time of the processor. Consequently, the designer should conform to a lower bandwidth for current control compared to the analog implementation of systems.

$$DPWM_s = \frac{V_{MO}(s)}{M(s)} = \frac{1}{2c_{pk}}\left(e^{-s(1-D)\frac{T_S}{2}} + e^{-s(1+D)\frac{T_S}{2}}\right) \quad (6)$$

$$\frac{1}{2}\left(e^{-s(1-D)\frac{T_S}{2}} + e^{-s(1+D)\frac{T_S}{2}}\right) = e^{-s\frac{T_S}{2}}\cos\left(w\frac{T_S}{2}D\right) \cong e^{-s\frac{T_S}{2}} \quad (7)$$

$$e^{-s\frac{T_S}{2}} \cong \frac{1-s\frac{T_S}{4}}{1+s\frac{T_S}{4}} \quad (8)$$

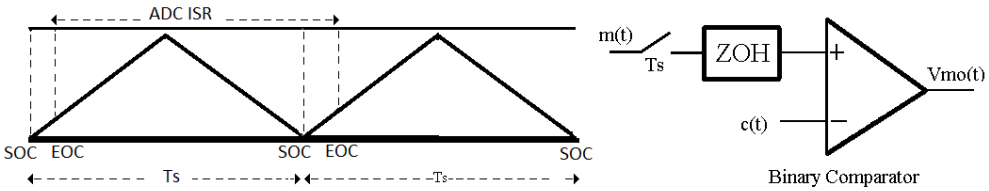

Fig. 3. Digital implementation of PWM and its s ynchronization with ADC

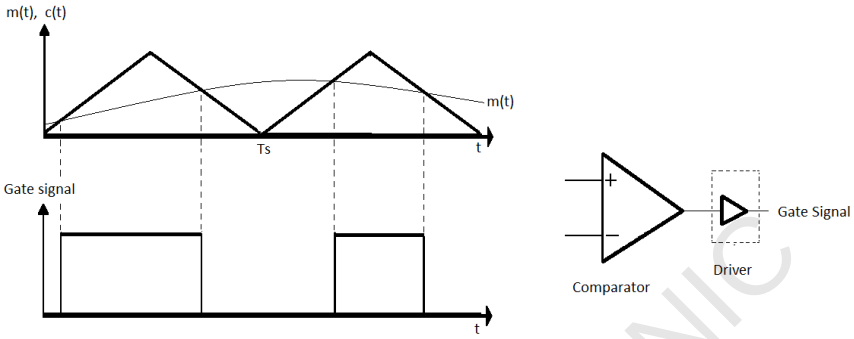

Fig. 4. Analog Implementation of PWM Modulation

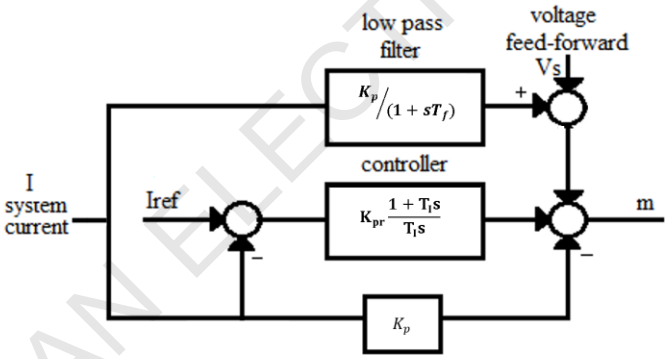

Fig. 5. The presented control schematic to eliminate the voltage sourced converter harmonic distortions

An increase in the switching frequency of the converters leads to a better harmonic elimination capability. On the other hand, the state-of-the-art switching devices such as Sic power MOSFETs have made the high-frequency switching possible. In summary, the limiting factor for the increase of switching frequency and conclusively the bandwidth of the current controller is the limited ISR time of the processor.

IV. IMPLEMENTED HARMONIC ELIMINATION METHOD

In order to eliminate high order harmonics from the current, the harmonic elimination method that the authors recently presented in [13] is utilized. A schematic of the implemented control method is depicted in Fig. 5. Compared to the conventional control method that employs resonant filters for compensation (equation 10), this architecture takes samples of system current and then, using a low pass filter, harmonics are filtered out from it and consequently they are again added to system current. In this way, harmonics distortions that have stemmed from grid voltage are eliminated. Therefore, effects of grid voltage harmonics are vanished. The corresponding transfer function for the implemented control architecture is expressed by the following equation:

$$G = K_p - \frac{Kp}{1+ST_f} = \frac{KpT_fS}{1+ST_f} \quad (9)$$

In equation 9, K_p is a gain employed to adjust the current feedback and feedforward. The pole in the equation 9 filters the high order harmonics, while the zero provides the

Fig. 6. The designed three phase rectifier

fundamental grid frequency dynamics in the terminal voltage. In equation 10, h is defined as the harmonic order and K_{ih} is the gain associated with the resonant filter of the harmonic h.

$$\sum_{h=5,7,11,13} \frac{2K_{ih}s}{s^2+(h\omega)^2} \quad (10)$$

TABLE I. PARAMETERS OF THE DESIGNED SYSTEM

PWM rectifier	
system rating	10 kw
Inductor L	1.5 mH
DC bus capacitor	1 mF
Switching frequency	20 KHz
Current controller speed	2 KHz
Voltage controller speed	10 Hz
Current loop sampling frequency	20 KHz
Voltage loop sampling frequency	5 KHz
DC link voltage	690 V
Phase grid voltage	400 V

V. SIMULATION AND EXPERIMENTAL RESULTS

This section verifies the proposed method for harmonic elimination with experimental results on the prototype rectifier, then time-domain simulations are conducted to observe the operation of the system under different circumstances and compares the benefits of the proposed method with the conventional methods that use selective harmonic elimination [10].

A. Experimental verification

The new control method for harmonic elimination is experimentally verified on a 10 kW three-phase PWM rectifier shown in Fig. 6, while digital control is implemented in the synchronous reference frame using a TMS320F28335 DSP. Table I shows the parameters of the designed three-phase PWM rectifier.

Fig. 7 compares the time between two succeeding ISR's for the proposed method and the method in [10]. The latter one is implemented with resonators on 300 Hz, 600 Hz, and 900 Hz in both d and q frames to compensate for 5th, 7th, 11th, 13th, 17th, and 19th harmonics. The required duration of ISR is 57μs which impels a maximum switching frequency of 15 kHz for the converter.

As shown in Fig. 7, with the proposed harmonic elimination method, the duration of ISR is 50 μs. The current waveform under this condition is shown in Fig. 8(c) which has a THD of 4.8%. The decrease of the processor burden is because of less complexity of harmonic elimination method which uses only a first-order low pass filter and a gain for the elimination of harmonics of all orders. Using the proposed harmonic compensation method, the processor is able to increase the switching frequency of the converter up to 20 kHz. Increasing the switching frequency allows better harmonic elimination.

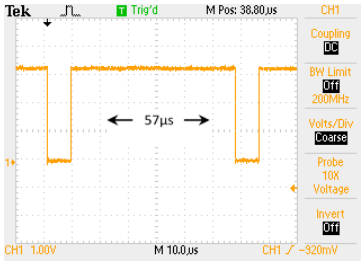

Fig. 7 (a)

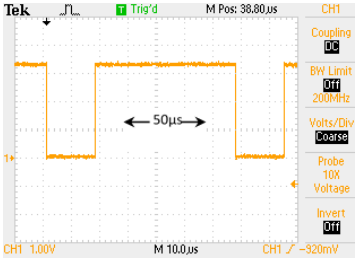

Fig. 7 (b)

Fig. 7. The process time for the current control loop. (a) With conventional harmonic elimination method presented by Bojoi et al. in [10] (b) With the proposed method

Fig. 8 (a)

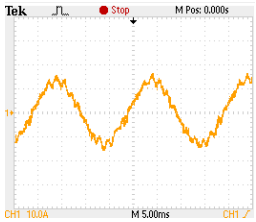

Fig. 8 (b)

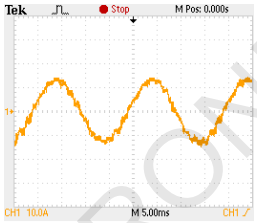

Fig. 8 (c)

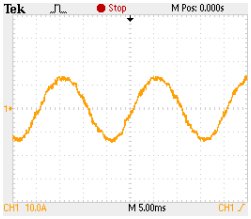

Fig. 8 (d)

Fig. 8 The grid current. (a) Without harmonic compensation at 15 KHz, and with the proposed harmonic elimination approach at (b) 10 KHz, (c) 15 KHz, (d) 20 KHz

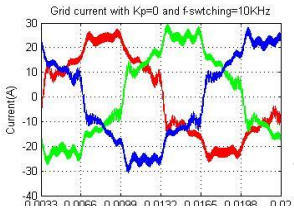

Fig. 9 (a)

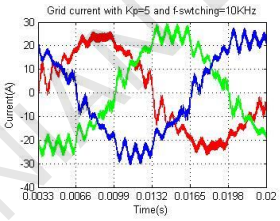

Fig. 9 (b)

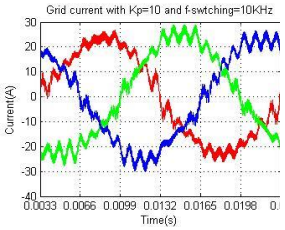

Fig. 9 (c)

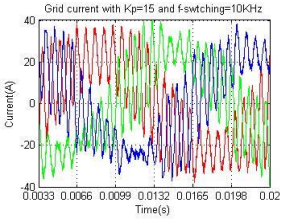

Fig. 9 (d)

Fig. 9, grid current with the proposed harmonic elimination method at $f_{switching} = 10\ KHz$ when grid voltage is polluted with 2 percent of each of the 5th, 7th, 11th, 13th, 17th, 19th, 21st, and 23rd order harmonics and; (a) K_p=0, (b) K_p=5, (c) K_p=10, (d) K_p=15,

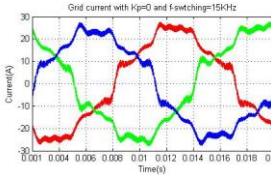

Fig. 10 (a)

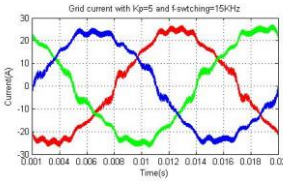

Fig. 10 (b)

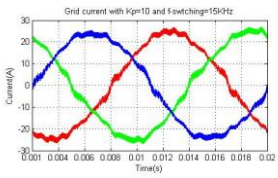

Fig. 10 (c)

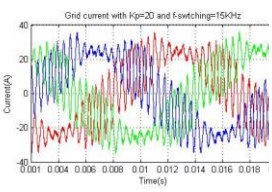

Fig. 10 (d)

Fig. 10 grid current with the proposed harmonic elimination method at $f_{switching} = 15\ KHz$ when grid voltage is polluted with 2 percent of each of the 5th, 7th, 11th, 13th, 17th, 19th, 21st, and 23rd order harmonics and ; (a) K_p=0, (b) K_p=5, (c) K_p=10, (d) K_p=20

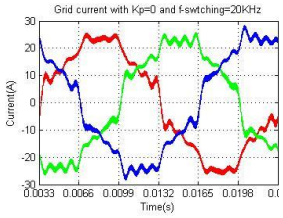

Fig. 11 (a)

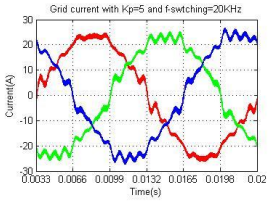

Fig. 11 (b)

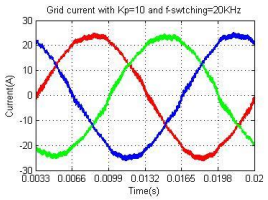

Fig. 11 (c)

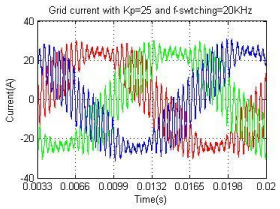

Fig. 11 (d)

Fig. 11, grid current with the proposed harmonic elimination method at $f_{switching} = 20\ KHz$ when grid voltage is polluted with 2 percent of each of the 5th, 7th, 11th, 13th, 17th, 19th, 21st, and 23rd order harmonics and; (a) K_p=0, (b) K_p=5, (c) K_p=10 , (d) K_p=20.

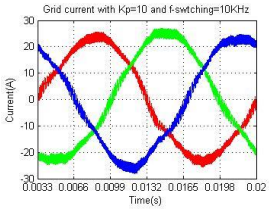

Fig. 12 (a)

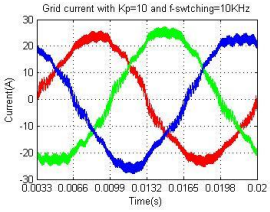

Fig. 12 (b)

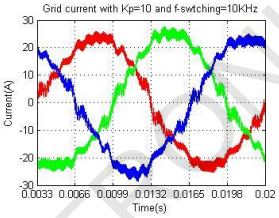

Fig. 12 (c)

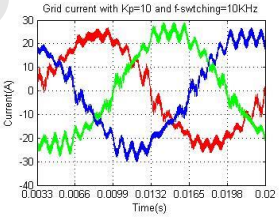

Fig. 12 (d)

Fig. 12 grid current with the proposed harmonic elimination method at $f_{switching} = 10\ KHz$ and K_p=10 when grid voltage is polluted with 2 percent of each of; (a) 5th, and 7th (b) 5th, 7th, 11th and 13th (c) 5th, 7th, 11th, 13th, 17th, and19th (d) 5th, 7th, 11th, 13th, 17th, 19th, 21st, and 23rd order harmonics.

TABLE II. COMPARISON OFEXPERIMENTAL RESULTS OBTAINED

	The Proposed method at 20KHz switching frequency	**The Proposed method at 15KHz switching frequency**	**The Proposed method at 10KHz**	**The Conventional method [10] at 15KHz**	**No harmonic elimination at 15Khz**
Current controller bandwidth	2kHz	1.5kHz	1kHz	1.5kHz	1.5kHz
Grid Voltage THD	2.5%	2.5%	2.5%	2.5%	2.5%
Grid Current THD	4%	4.8%	9%	4.8%	18%

Therefore, the compensator is able to compensate for higher-order harmonics such as 21st, and 23rd. Fig. 8(d) shows the grid current under this condition which has a THD of 4%.

For better clarification of the effect of switching frequency and bandwidth on the elimination of current harmonics, the proposed method was applied to a rectifier system with the switching frequency at 10 kHz. With proper tuning of the gain K_p in Equation 9, with the grid voltage THD of 2.5%, the observed current THD was 9%. The corresponding waveform of the grid current under this condition is shown in Fig. 8(b). Fig. 8(a) shows the current waveform while no harmonic elimination method is applied. Under this condition, the measured current THD is 19%. The measured experimental results are summarized in Table II.

B. Simulation verification

In order to verify the effectiveness of the proposed harmonic elimination method, simulations are carried out with three different switching frequencies, i.e. 10 kHz, 15 kHz, and 20 kHz while the proposed harmonic elimination method being applied.

Fig. 9(a) to Fig. 9(d) show the grid current with the switching frequency at 10 kHz while 2% pollution of each of the 5th, 7th, 11th, 13th, 17th, 19th, 21st, and 23rd order harmonics are added to the grid voltage. By increasing the gain K_p up to the stability limit, high order harmonics are not eliminated, as the bandwidth is not large enough to cover them. Fig. 12(a) shows the grid current at the switching frequency of 10 kHz while the grid voltage pollution of each 5th and 7th order harmonics being added by 2%. In this condition, by properly tuning the gain K_p , the harmonics are eliminated successfully. Fig. 12(b), Fig. 12(c), and Fig. 12(d) show the grid current while the grid voltage is polluted by 2% of each of higher-order harmonics of 5th, 7th, 11th, 13th, and 5th, 7th, 11th, 13th, 17th, 19th, and 5th, 7th, 11th, 13th, 17th, 19th, 21st, and 23rd respectively. Under these conditions, the harmonic elimination effect diminishes increasingly. This is due to the fact that 10 kHz of switching frequency forces a bandwidth to the controller which is not fast enough to compensate higher-order harmonics.

Fig. 10(a) to Fig. 10(f) show the grid current with the switching frequency at 15 kHz while the grid voltage pollution of each of the 5th, 7th, 11th, 13th, 17th, 19th, 21st, and 23rd order harmonics are added by 2% and Fig. 11(a) to Fig 11(f) show the grid current under the same grid condition but at 20 kHz. Best elimination of harmonics occurs at $K_p = 20$ with switching frequency at 20 kHz. This is due to the fact that this switching frequency, compared to 10 kHz and 15 kHz, provides a larger bandwidth for the current controller.

VI. CONCLUSION

For harmonic elimination, this paper presented a new approach that simplifies the computation effort of the processor and has a better performance compared to the conventional harmonic elimination approaches. The proposed method takes samples of system current and then, using a low pass filter, harmonics are filtered out from it and consequently they are added to system current. Experiment results showed that the proposed method for harmonic elimination leads to less computation effort for the processor. Therefore, the switching frequency of the converter was increased by 5 KHz that resulted in a faster current controller. The wider bandwidth allowed to compensate for higher-order harmonics, which improved harmonic elimination capability by 0.8% in comparison to typical harmonic elimination approaches under the same grid conditions.

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